Supplementary Material for Improving Multicore Server Performance and Reducing Energy Consumption by Workload Dependent Dynamic Power Management

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TABLE 1 Summary of Notations

Sa multicore server processormnumber of cores λ task arrival ratertask arrival ratertask execution requirementscore execution speed x task execution time μ the average service rate ρ core utilization p_k the probability that there are k tasks in Sknumber of tasks waiting or being processed P_g the probability of queueing N the average number of tasks in S T the average task response time P dynamic power consumptionwan activity factor C the loading capacitance V the supply voltagefthe clock frequency α an exponent such that $P \propto s^{\alpha}$ P^* static power dissipation μ_k workload dependent core execution speed ρ_k workload dependent core utilization (c,d) an arithmetic-speed scheme $s_k = qa^k$ (b, s_1, s_2) a two-speed scheme \vec{P} power constraint		
mnumber of cores λ task arrival rate r task arrival rate r task execution requirement s core execution speed x task execution time μ the average service rate ρ core utilization p_k the probability that there are k tasks in S k number of tasks waiting or being processed P_q the probability of queueing N the average number of tasks in S T the average task response time P dynamic power consumption w an activity factor C the loading capacitance V the supply voltage f the clock frequency α an exponent such that $P \propto s^{\alpha}$ P^* static power dissipation μ_k workload dependent core execution speed ρ_k workload dependent core utilization (c,d) an arithmetic-speed scheme $s_k = qa^k$ (b, s_1, s_2) a two-speed scheme P power constraint	Notation	Definition
$ \begin{array}{cccc} \lambda & \mbox{task arrival rate} \\ r & \mbox{task arrival rate} \\ r & \mbox{task execution requirement} \\ s & \mbox{core execution speed} \\ x & \mbox{task execution time} \\ \mu & \mbox{the average service rate} \\ \rho & \mbox{core utilization} \\ p_k & \mbox{the probability that there are } k \mbox{tasks in } S \\ h & \mbox{number of tasks waiting or being processed} \\ P_g & \mbox{the probability of queueing} \\ N & \mbox{the average number of tasks in } S \\ T & \mbox{the average number of tasks in } S \\ T & \mbox{the average task response time} \\ P & \mbox{dynamic power consumption} \\ w & \mbox{an activity factor} \\ C & \mbox{the loading capacitance} \\ V & \mbox{the supply voltage} \\ f & \mbox{the clock frequency} \\ \alpha & \mbox{an exponent such that } P \propto s^{\alpha} \\ P^* & \mbox{static power dissipation} \\ \mu_k & \mbox{workload dependent core execution speed} \\ \rho_k & \mbox{workload dependent core utilization} \\ (c, d) & \mbox{an arithmetic-speed scheme } s_k = c + kd \\ (q, a) & \mbox{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \mbox{a two-speed scheme} \\ p & \mbox{power constraint} \\ \end{array} $		a multicore server processor
r task execution requirement s core execution speed x task execution time μ the average service rate ρ core utilization p_k the probability that there are k tasks in S k number of tasks waiting or being processed P_q the probability of queueing N the average number of tasks in S T the average task response time P dynamic power consumption w an activity factor C the loading capacitance V the supply voltage f the clock frequency α an exponent such that $P \propto s^{\alpha}$ P^* static power dissipation μ_k workload dependent task service rate $workload$ dependent core execution speed ρ_k a geometric-speed scheme $s_k = c + kd$ (q, a) a geometric-speed scheme $s_k = qa^k$ \tilde{P} power constraint	m	number of cores
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	λ	task arrival rate
$ \begin{array}{cccc} x & \mbox{task execution time} \\ \mu & \mbox{the average service rate} \\ \rho & \mbox{core utilization} \\ p_k & \mbox{the probability that there are }k \mbox{tasks in }S \\ k & \mbox{number of tasks waiting or being processed} \\ P_g & \mbox{the probability of queueing} \\ N & \mbox{the average number of tasks in }S \\ T & \mbox{the average task response time} \\ P & \mbox{dynamic power consumption} \\ w & \mbox{an activity factor} \\ C & \mbox{the loading capacitance} \\ V & \mbox{the supply voltage} \\ f & \mbox{the clock frequency} \\ \alpha & \mbox{an exponent such that }P \propto s^{\alpha} \\ P^* & \mbox{static power dissipation} \\ \mu_k & \mbox{workload dependent task service rate} \\ s_k & \mbox{workload dependent core utilization} \\ (c,d) & \mbox{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \mbox{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \mbox{a two-speed scheme} \\ \hline \end{array} $	r	task execution requirement
$ \begin{array}{cccc} \mu & \text{the average service rate} \\ \rho & \text{core utilization} \\ p_k & \text{the probability that there are } k \text{ tasks in } S \\ k & \text{number of tasks waiting or being processed} \\ P_g & \text{the probability of queueing} \\ N & \text{the average number of tasks in } S \\ T & \text{the average number of tasks in } S \\ T & \text{the average task response time} \\ P & \text{dynamic power consumption} \\ w & \text{an activity factor} \\ C & \text{the loading capacitance} \\ V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c,d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \text{a two-speed scheme} \\ P & \text{power constraint} \\ \end{array} $	s	core execution speed
$ \begin{array}{c c} \rho & \text{core utilization} \\ p_k & \text{the probability that there are } k \text{ tasks in } S \\ k & \text{number of tasks waiting or being processed} \\ P_g & \text{the probability of queueing} \\ N & \text{the average number of tasks in } S \\ T & \text{the average number of tasks in } S \\ T & \text{the average task response time} \\ P & \text{dynamic power consumption} \\ w & \text{an activity factor} \\ C & \text{the loading capacitance} \\ V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c,d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \text{a two-speed scheme} \\ P & \text{power constraint} \\ \end{array} $	x	task execution time
$ \begin{array}{cccc} p_k & \text{the probability that there are } k \text{ tasks in } S \\ k & \text{number of tasks waiting or being processed} \\ P_q & \text{the probability of queueing} \\ \hline N & \text{the average number of tasks in } S \\ \hline T & \text{the average number of tasks in } S \\ \hline T & \text{the average task response time} \\ \hline P & \text{dynamic power consumption} \\ w & \text{an activity factor} \\ \hline C & \text{the loading capacitance} \\ \hline V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ \hline P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c,d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ \hline P & \text{power constraint} \\ \end{array} $	μ	
$ \begin{array}{cccc} k & \text{number of tasks waiting or being processed} \\ P_g & \text{the probability of queueing} \\ \hline N & \text{the average number of tasks in } S \\ \hline T & \text{the average number of tasks in } S \\ \hline T & \text{the average task response time} \\ \hline P & \text{dynamic power consumption} \\ w & \text{an activity factor} \\ \hline C & \text{the loading capacitance} \\ \hline V & \text{the supply voltage} \\ \hline f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ \hline P^* & \text{static power dissipation} \\ \hline \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \hline \rho_k & \text{workload dependent core utilization} \\ \hline (c,d) & \text{an arithmetic-speed scheme } s_k = qa^k \\ \hline (b,s_1,s_2) & \text{a two-speed scheme} \\ \hline P & \text{power constraint} \\ \end{array} $	ρ	
$\begin{array}{cccc} P_{g} & \text{the probability of queueing} \\ N & \text{the average number of tasks in } S \\ T & \text{the average task response time} \\ P & \text{dynamic power consumption} \\ w & \text{an activity factor} \\ C & \text{the loading capacitance} \\ V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^{*} & \text{static power dissipation} \\ \mu_{k} & \text{workload dependent task service rate} \\ s_{k} & \text{workload dependent core execution speed} \\ \rho_{k} & \text{workload dependent core utilization} \\ (c, d) & \text{an arithmetic-speed scheme } s_{k} = c + kd \\ (q, a) & \text{a two-speed scheme} \\ \bar{P} & \text{power constraint} \\ \end{array}$		the probability that there are k tasks in S
$ \begin{array}{cccc} T & \text{the average task response time} \\ P & \text{dynamic power consumption} \\ w & \text{an activity factor} \\ C & \text{the loading capacitance} \\ V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c, d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q, a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \text{a two-speed scheme} \\ \bar{P} & \text{power constraint} \\ \end{array} $		number of tasks waiting or being processed
$ \begin{array}{cccc} T & \text{the average task response time} \\ P & \text{dynamic power consumption} \\ w & \text{an activity factor} \\ C & \text{the loading capacitance} \\ V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c, d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q, a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \text{a two-speed scheme} \\ \bar{P} & \text{power constraint} \\ \end{array} $	P_q	the probability of queueing
$ \begin{array}{cccc} P & & & & & & \\ dynamic power consumption \\ w & & & & \\ an activity factor \\ C & & & & & \\ the loading capacitance \\ V & & & & & \\ the supply voltage \\ f & & & & \\ the clock frequency \\ \alpha & & & & & \\ an exponent such that P \propto s^{\alpha} \\ P^* & & & & \\ static power dissipation \\ \mu_k & & & & \\ workload dependent task service rate \\ workload dependent core execution speed \\ \rho_k & & & & \\ workload dependent core utilization \\ (c,d) & & & \\ an arithmetic-speed scheme \\ (g,a) & & & \\ (b,s_1,s_2) & & \\ a two-speed scheme \\ \bar{P} & & \\ power constraint \\ \end{array} $		the average number of tasks in S
$ \begin{array}{cccc} w & \text{an activity factor} \\ C & \text{the loading capacitance} \\ V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c, d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q, a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \text{a two-speed scheme} \\ \bar{P} & \text{power constraint} \\ \end{array} $		
$ \begin{array}{cccc} w & \text{an activity factor} \\ C & \text{the loading capacitance} \\ V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c, d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q, a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b, s_1, s_2) & \text{a two-speed scheme} \\ \bar{P} & \text{power constraint} \\ \end{array} $	P	dynamic power consumption
$ \begin{array}{cccc} V & \text{the supply voltage} \\ f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c,d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & \text{a two-speed scheme} \\ \bar{P} & \text{power constraint} \end{array} $		an activity factor
$ \begin{array}{cccc} f & \text{the clock frequency} \\ \alpha & \text{an exponent such that } P \propto s^{\alpha} \\ P^* & \text{static power dissipation} \\ \mu_k & \text{workload dependent task service rate} \\ s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c,d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & \text{a two-speed scheme} \\ \tilde{P} & \text{power constraint} \end{array} $		the loading capacitance
$ \begin{array}{c cccc} \alpha & \text{ an exponent such that } P \propto s^{\alpha} \\ P^* & \text{ static power dissipation} \\ \mu_k & \text{ workload dependent task service rate} \\ s_k & \text{ workload dependent core execution speed} \\ \rho_k & \text{ workload dependent core utilization} \\ (c,d) & \text{ an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{ a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & \text{ a two-speed scheme} \\ \tilde{P} & \text{ power constraint} \end{array} $		
$ \begin{array}{c cccc} P^* & \mbox{static power dissipation} \\ \mu_k & \mbox{workload dependent task service rate} \\ s_k & \mbox{workload dependent core execution speed} \\ \rho_k & \mbox{workload dependent core utilization} \\ (c,d) & \mbox{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \mbox{a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & \mbox{a two-speed scheme} \\ \tilde{P} & \mbox{power constraint} \end{array} $	$\int f$	the clock frequency
$ \begin{array}{ccc} \mu_k & & \text{workload dependent task service rate} \\ s_k & & \text{workload dependent task service rate} \\ \rho_k & & \text{workload dependent core execution speed} \\ \rho_k & & \text{workload dependent core utilization} \\ (c,d) & & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & & \text{a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & & \text{a two-speed scheme} \\ \bar{P} & & \text{power constraint} \end{array} $		an exponent such that $P \propto s^{lpha}$
$ \begin{array}{c c} s_k & \text{workload dependent core execution speed} \\ \rho_k & \text{workload dependent core utilization} \\ (c,d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & \text{a two-speed scheme} \\ \tilde{P} & \text{power constraint} \end{array} $	P^*	static power dissipation
$ \begin{array}{c c} \rho_k & \text{workload dependent core utilization} \\ (c,d) & \text{an arithmetic-speed scheme } s_k = c + kd \\ (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & \text{a two-speed scheme} \\ \tilde{P} & \text{power constraint} \end{array} $	μ_k	workload dependent task service rate
$ \begin{array}{c c} (c,d) \\ (q,a) \\ (b,s_1,s_2) \\ \tilde{P} \\ \tilde{P} \end{array} \begin{array}{c} \text{an arithmetic-speed scheme } s_k = c + kd \\ \text{a geometric-speed scheme } s_k = qa^k \\ \text{a two-speed scheme} \\ \text{power constraint} \end{array} $	s_k	
$ \begin{array}{ c c c } (q,a) & \text{a geometric-speed scheme } s_k = qa^k \\ (b,s_1,s_2) & \text{a two-speed scheme} \\ \tilde{P} & \text{power constraint} \end{array} $	ρ_k	workload dependent core utilization
$ \begin{array}{c c} (b, s_1, s_2) \\ \tilde{P} \\ \tilde{P} \end{array} \text{a two-speed scheme} \\ \text{power constraint} \end{array} $	(c,d)	an arithmetic-speed scheme $s_k = c + kd$
<i>P</i> power constraint		a geometric-speed scheme $s_k = qa^k$
<i>P</i> power constraint	(b, s_1, s_2)	a two-speed scheme
\tilde{T} performance constraint	$ $ \tilde{P}	power constraint
	$ $ \tilde{T}	performance constraint

1 NOTATIONS

For reader's convenience, we provide Table 1, which gives a summary of notations and their definitions in the order introduced in the paper.

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2 PROOFS OF THEOREMS AND COROLLAR-IES

Theorem 1: A speed scheme $(s_1, s_2, s_3, ...)$ is valid if and only if the summation

$$\sum_{k=m}^{\infty} \rho_1 \rho_2 \cdots \rho_k$$

converges.

Proof. It is clear that

$$p_k = \begin{cases} p_0 \frac{m^k}{k!} \cdot \rho_1 \rho_2 \cdots \rho_k, & 1 \le k \le m-1; \\ p_0 \frac{m^m}{m!} \cdot \rho_1 \rho_2 \cdots \rho_k, & k \ge m; \end{cases}$$

where

$$p_0 = \left(1 + \sum_{k=1}^{m-1} \frac{m^k}{k!} \cdot \rho_1 \rho_2 \cdots \rho_k + \frac{m^m}{m!} \sum_{k=m}^{\infty} \rho_1 \rho_2 \cdots \rho_k\right)^{-1}$$

Therefore, for a fixed m, $p_0 > 0$ if and only if

$$\sum_{k=m}^{\infty} \rho_1 \rho_2 \cdots \rho_k$$

converges.

Corollary 1: If there is some $n \ge 1$, such that $\rho_k < 1$ for all $k \ge n$, then a speed scheme $(s_1, s_2, s_3, ...)$ is valid.

Proof. Without loss of generality, we assume that $n \ge m$. It is clear that

$$\sum_{k=m}^{\infty} \rho_1 \rho_2 \cdots \rho_k$$

converges if and only if

$$\sum_{k=n}^{\infty} \rho_1 \rho_2 \cdots \rho_k$$

converges. Let $\rho = \max\{\rho_n, \rho_{n+1}, ...\}$. Then,

$$\sum_{k=n}^{\infty} \rho_1 \rho_2 \cdots \rho_k < \sum_{k=n}^{\infty} \rho^k = \frac{\rho^n}{1-\rho},$$

and

$$\sum_{k=n}^{\infty} \rho_1 \rho_2 \cdots \rho_k$$

converges.

Corollary 2: Any arithmetic-speed scheme with $c > \lambda \bar{r}/m$ or d > 0 is valid.

Proof. It is clear that

$$\rho_k = \frac{\lambda \bar{r}}{m(c+kd)}$$

and $\rho_k < 1$ for all $k \ge n$, where

$$n = \left\lceil \frac{1}{d} \left(\frac{\lambda \bar{r}}{m} - c \right) \right\rceil$$

The result follows Corollary 1.

Corollary 3: Any geometric-speed scheme with $q > \lambda \bar{r}/m$ or a > 1 is valid.

Proof. It is clear that

$$\rho_k = \frac{\lambda \bar{r}}{mqa^k},$$

and $\rho_k < 1$ for all $k \ge n$, where

$$n = \left\lceil \log_a \frac{\lambda \bar{r}}{mq} \right\rceil$$

The result follows Corollary 1.

Corollary 4: Any two-speed scheme with $\rho_2 < 1$ is valid.

Proof. The result follows Corollary 1 immediately by taking n = b + 1.

3 A NUMERICAL METHOD AND EXAMPLES OF POWER CONSUMPTION REDUCTION

In Table 2, we show numerical data for an optimal two-speed scheme, with the same parameter setting as Table 9 of the main paper. We observe that there is an optimal choice of (s_1, s_2) , such that a two-speed scheme with a given *b* is optimized, in the sense that the power consumption *P* is minimized, while the average task response time is no more than (actually fixed at) *T*.

To minimize $P(s_1, s_2)$ subject to the constraint $T(s_1, s_2) = \tilde{T}$, we need to find s_1 , s_2 , and ϕ such that

$$\frac{\partial P}{\partial s_i} = \phi \frac{\partial T}{\partial s_i},$$

for i = 1, 2, that is,

$$\phi = \frac{s_1}{M_1} = \frac{s_2}{M_2},$$

TABLE 2 Numerical Data for Optimal Two-Speed Schemes

	Idle-Spe	ed Model	Constant-Speed Model					
s_1	s_2 P		\$2 82	P				
T = 0.80								
1.20	4.7123790	90.5475024	4.7123790	91.4555628				
1.25	3.5422746	63.1557243	3.5422746	64.2889058				
1.30	2.9545801	52.6442432	2.9545801	54.0465778				
1.35	2.6021857	47.5959053	2.6021857	49.3174316				
1.40	2.3680850	44.9321569	2.3680850	47.0293046				
1.45	2.2018070	43.5171008	2.2018070	46.0530438				
1.50	2.0780066	42.8445489	2.0780066	45.8895223				
1.55	1.9825587	42.6583950	1.9825587	46.2899715				
1.60	1.9069675	42.8166746	1.9069675	47.1199978				
1.65	1.8458156	43.2350867	1.8458156	48.3030594				
T = 1.00								
1.15	2.0056416	41.8051046	2.0056416	42.2728288				
1.20	1.9509196	40.8553629	1.9509196	41.4690733				
1.25	1.9022092	40.1691893	1.9022092	40.9637048				
1.30	1.8587553	39.7134783	1.8587553	40.7293344				
1.35	1.8199114	39.4620199	1.8199114	40.7459277				
1.40	1.7851217	39.3939612	1.7851217	40.9992359				
1.45	1.7539062	39.4926306	1.7539062	41.4795854				
1.50	1.7258491	39.7446313	1.7258491	42.1809280				
1.55	1.7005890	40.1391357	1.7005890	43.1000900				
1.60	1.6778107	40.6673325	1.6778107	44.2361683				
		T = 1.2	0					
1.10	1.7580956	38.7306356	1.7580956	38.9891602				
1.15	1.7394136	38.3625219	1.7394136	38.7143489				
1.20	1.7213085	38.0911069	1.7213085	38.5623417				
1.25	1.7038463	37.9193108	1.7038463	38.5412141				
1.30	1.6870797	37.8494471	1.6870797	38.6589762				
1.35	1.6710477	37.8832801	1.6710477	38.9236095				
1.40	1.6557767	38.0220867	1.6557767	39.3430968				
1.45	1.6412811	38.2667167	1.6412811	39.9254430				
1.50	1.6275646	38.6176489	1.6275646	40.6786837				
1.55	1.6146217	39.0750405	1.6146217	41.6108811				

TABLE 3

Numerical Data for Two-Speed Scheme Optimization

	Idle-Speed Model			Constant-Speed Model		
\tilde{T}	s_1	s_2	P	s_1	s_2	P
0.80	1.5494532	1.9834831	42.6583747	1.4872276	2.1064988	45.8703958
1.00	1.3946833	1.7886433	39.3930141	1.3214688	1.8415463	40.7066639
1.20	1.3087933	1.6842061	37.8478401	1.2329176	1.7097364	38.5332143

where M_1 and M_2 are given in Section 5.1 of the main paper. We use a numerical method similar to that in Section 5.3 of the main paper, with the following differences. First, we can find s_2 such that $T(s_1, s_2) = \tilde{T}$ by using the classic bisection method and the fact that $T(s_1, s_2)$ is a decreasing function of s_2 . Second, we notice that $\Delta(s_1) = s_1/M_1 - s_2/M_2$ is a decreasing function of s_1 along the path $T(s_1, s_2) = \tilde{T}$.

In Table 3, we display our optimal two-speed schemes with m = 7, $P^* = 2$, $\lambda = 10$, $\bar{r} = 1$, and b = 10, for both idle-speed and constant-speed models, where $\tilde{T} = 0.8, 1.0, 1.2$.

4 FURTHER RESEARCH DIRECTIONS

We would like to point out that our optimal twospeed scheme problem can be extended to include bas a variable. However, since b is a discrete variable, there hardly exists an analytical solution.

Furthermore, two-speed schemes can be generalized to *d*-speed schemes.

Definition. In a *d-speed scheme* with parameters $(b_1, b_2, ..., b_{d-1}, s_1, s_2, ..., s_d)$, where $b_1 < b_2 < \cdots < b_{d-1}$, the speed of the *m* cores is s_1 when there are $k \leq b_1$ tasks, and s_2 when there are $b_1 + 1 \leq k \leq b_2$ tasks, ..., and s_{d-1} when there are $b_{d-2} + 1 \leq k \leq b_{d-1}$ tasks, and s_d when there are $k \geq b_{d-1} + 1$ tasks.

Our optimization problem for two-speed schemes can be generalized to *d*-speed schemes, i.e., to minimize *T* by choosing *d*, $b_1, b_2, ..., b_{d-1}$, and $s_1, s_2, ..., s_d$, subject to the constraint that the total power consumption does not exceed *P*. Although closed-form expressions of *T* and *P* can be figured out, the numerical procedures will be more involved.

Of course, our ultimate open problem is to find an optimal speed scheme $(s_1, s_2, s_3, ...)$ such that the performance is optimized with a power constraint or the power is minimized with a performance constraint.

Finally, it is of practical importance to incorporate the technique of workload dependent dynamic power management into real servers in cloud computing and data centers to improve server performance and to reduce energy consumption.